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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/036,020	
		Filing Date	12/26/2001	
		First Named Inventor	Sailesh Chittipeddi	
		Group Art Unit	2812	
		Examiner Name	Unassigned	
2	of	2	Attorney Docket Number	Chittipeddi 89-14

OTHER PRIOR ART - NONPATENT LITERATURE DOCUMENTS			
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
BR	AA	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.	
BR	BB	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.	
BR	CC	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.	
BR	DD	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEDM 1988, pp. 222-225.	
BR	EE	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", Technical Digest of IEDM, 1999, pp. 75-78.	
BR	FF	OH, ET AL, "50 nm Vertical Replacement-Gate (VRG) pMOSFETs", IEEE 2000.	
BR	GG	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A High-Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document.	
BR	HH	MONROE, ET AL, "The Vertical, Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.	
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Examiner Signature	Behar K. Kerman	Date Considered	07/28/2003.
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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